CCD Camera

I. CCD Camera Operation: Solid State Physics

A. MOS Capacitor Gate

The basic component of a CCD pixel is a Metal-Oxide-Semiconductor (MOS) capacitor. MOS capacitors are of two types: surface and buried channel. They differ mainly in their fabrication.[1] The buried channel capacitor is the most common capacitor. The subsequent discussion will focus on this type of capacitor.

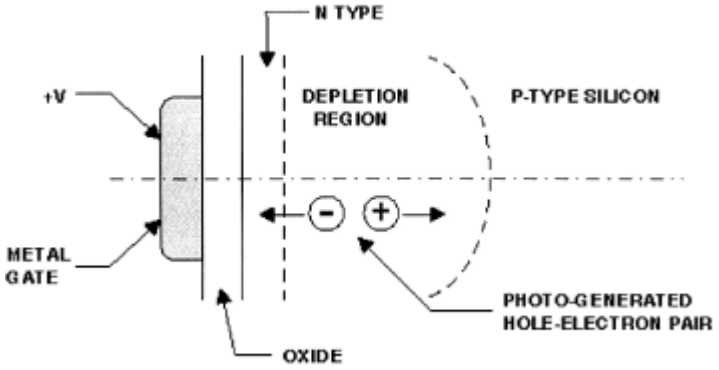

Figure 1. Buried Channel MOS capacitor.[34] Electrons migrate towards the N-Type region and holes migrate to the P-type region. The gate creates an electric field, which attracts more electrons into the N-type substrate.

The entire capacitor is based on a P-type substrate layer. This provides the "holes" for which free electrons can occupy. An N-type substrate, about 1 μm thick, which provides the electrons, is formed on the surface of the p-type substrate. (See figure 1).

A non-conductive oxide layer, approximately 0.1 μm thick acts as the barrier forming the separating channel between the two gates of a capacitor. Finally, a metallic gate serves to bias the entire capacitor.

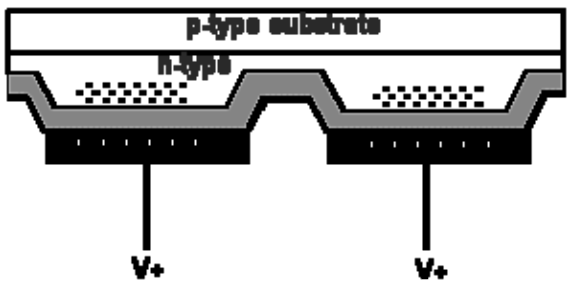

Figure 2. When a bias voltage is applied to the gates, electrons are pulled into the wells and charge cannot flow between adjoining gates. The gray region is the non-conductive oxide barrier.

When photons interact with the p-doped substrate, electron-hole pairs are generated forming a depletion region. Each gate is effectively surrounded by the non-conductive oxide barrier such that the electron charge accumulated at the gate and the n-type substrate barrier sits in a so-called well. When the gate is at a positive potential, more of the photoelectrically generated electrons gather closer to the gate. Each potential is therefore separated from its neighbor because charge does not move from one gate to the next while the biasing gate is high (see figure 2)

Rudimentary descriptions of P-type and N-type semiconductors can be found via Wikipedia at:
http://en.wikipedia.org/wiki/P-type_semiconductor
http://en.wikipedia.org/wiki/N-type_semiconductor

B. CCD Pixel

Many configurations exist for combining gates to make a pixel. The most common practice for fabricating CCD pixels is the three phase structure illustrated in figure 3. Each CCD pixel is composed of three MOS gate capacitors. Each pixel, as well as each gate, is separated by the non-conductive oxide barrier labeled as channel stop in figure 3. The three phase pixel is the most popular because it has higher yield as well as higher process tolerance for this type of fabrication technology.

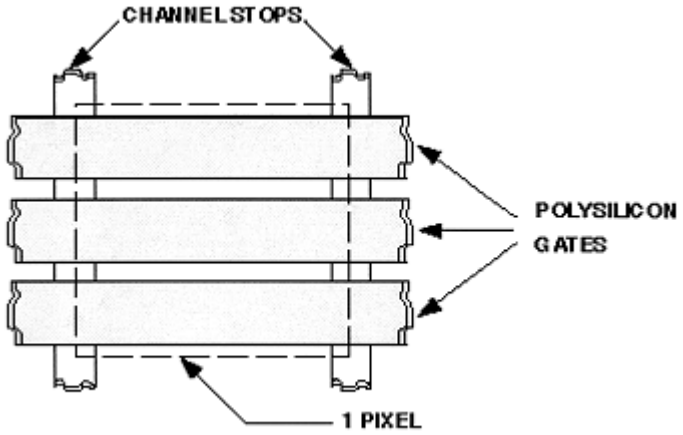

Figure 3. A typical CCD Pixel is composed of three MOS capacitors.[34] The hashed line represents a single pixel. The channel stops are the non-conductive oxide barrier.

II. CCD Camera Operation: Charge Transfer

A. Charge Transfer between gates and pixels

The quantity of charge collected in a well is linearly proportional to the photon flux incident on the capacitor in addition to the amount of time the element is exposed. Figure 4 shows the quantum efficiency for a typical CCD camera. The detector has a maximum sensitivity for incident wavelengths between 600 and 700 nm which translates into a maximal electron production in each gate. Collecting light in this range will ensure the highest signal to noise ratio the camera is capable of achieving.

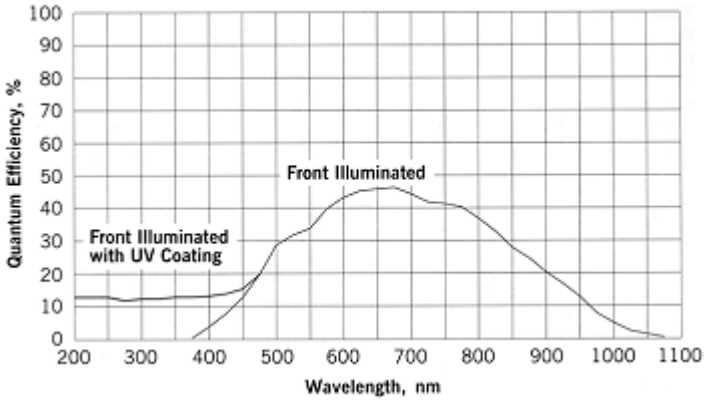

Figure 4. Quantum Efficiency of a typical CCD array.[28] Di-4-ANNEPS emission spectrum closely matches the CCD's quantum efficiency.

When a pixel is ready for recording, the center gate's potential is raised to +5 Volts and the surrounding gates are set to a zero potential. This way, any charge generated in the center gate or its two surrounding gates diffuses into the center gate's well. When the camera is ready to move the charge across the array, the center gate is allowed to go to the zero potential while the third gate is raised. The electrons previously trapped in the center gate are now free to diffuse to the new local minimum occurring under the third gate. A timing diagram is provided in figure 5. This transfer scheme continues across the entire array until the charge from each element is read off. The terminology "charge coupled" arises from this transfer of charge from one gate to another.

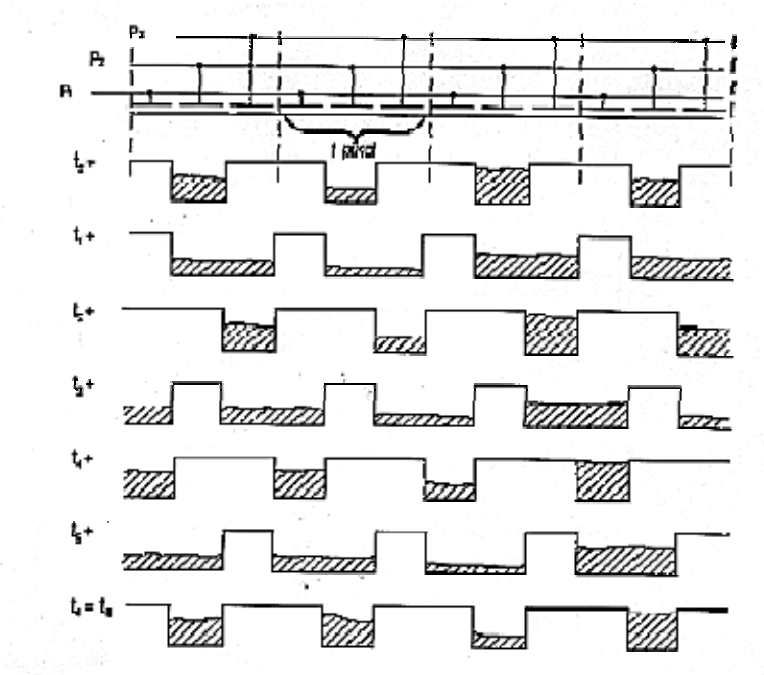

Figure 5. Three phase charge timing process.[34] The time t_2+ corresponds to the time capacitor 2 is high. Likewise t_3+ corresponds to the time that capacitor 3 is high. This pattern is repeated until the entire array is read off.

B. Frame Transfer Technology

Many CCD cameras do not sue mechanical shutters. If a mechanical shutter is not used to precisely quantify the start and finish of a single frame, light collection continues uninterrupted. In order to minimize the lag between the light collected by the first pixel read to the last pixel read, frame transfer technology was created. The hardware rate limiting step is the A/D converter. As such, frame transfer allows one half of an array to collect light continuously while the other half of the array is digitized. The half of the array that is digitized is covered by an opaque substance called a mask. Figure 6 is a schematic representation of how a frame transfer camera works. Readout of the frame transfer half of the array (the shaded region) begins with the simultaneous shifting of all pixels one column towards the shift register (the separate column on the right). The shift register is a line of pixels along one side of a CCD array, not sensitive to light and used only for readout. The charge in the shift register is then shifted to the A/D converter (the box in the lower right corner of each panel). Once the shift register is emptied, the entire process of shifting the charge on the entire array over towards the shift register is repeated. When the covered half of the array has been fully digitized, the exposed half of the array is transferred at very high speeds, on the order of 1 μsec/column into the frame transfer half of the array. An exposed half of the array can be transferred to the mask region in under 0.288 msec.

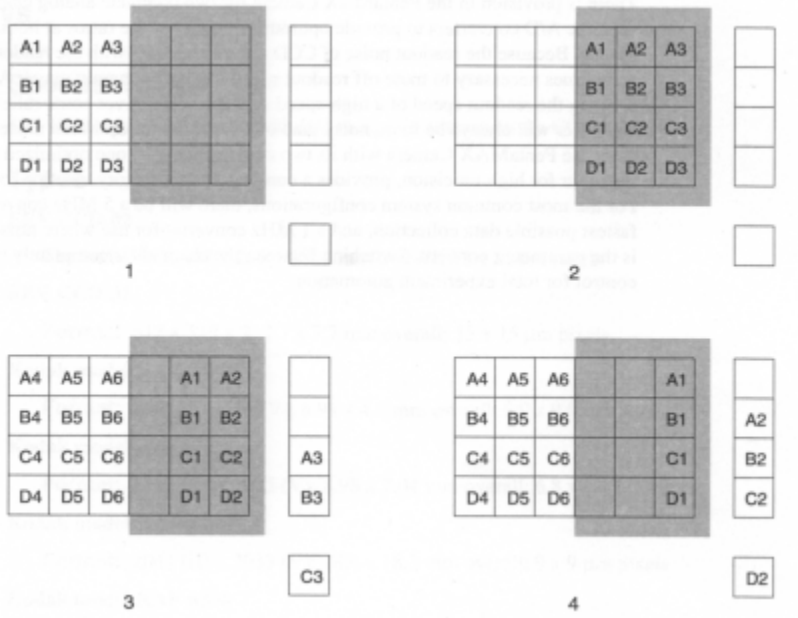

Figure 6. Representation of Frame Transfer operation[29] The gray region represents the covered half (frame transfer half) of the array. The frame transfer half is read off in its entirety before the exposed half of the array is transferred over.

The main advantages of a Frame Transfer (FT) Camera are:[2]

1. Light collection is continuous
2. Light collection and readout are simultaneous thus offering higher frame rates
3. A mechanical shutter is not required, reducing the chance of mechanical failure and allowing for faster operation
4. Two images can be taken in rapid succession

The disadvantages are that the imaging area is smaller then using the entire chip because one half of the array is masked. Instead of collecting from 576x384 pixels, the array size is reduced to 288 x 384 pixels. Furthermore, skew and smearing are inherent problems of the CCD. The skew refers to the actual point in time the first pixel corresponds to, relative to the point in time the last pixel was recorded.

A CCD element is an integrating device because it is continually collecting light. When a charge is moved from one pixel to another, a small amount of charge is added at each pixel sight equal to an exposure of 1μsec. This occurs for every pixel. Therefore, the pixels in the last column are subjected to 368 μsec of light that does not originate at the recording site. This apparent discrepancy is called smear. Fortunately, the light collected during the full exposure time is much greater than the light collected during transfer. Integration also causes a smearing of an edge. A step input will yield a ramp output as would be expected from an integrating device. The slope of the ramp is inversely proportional to the integration (exposure) time.

III. CCD Camera Operation: Control

A. The PCI Board

The PCI interface board connected to a PC controls the camera operation and serves as the data buffer (see figure 7). A high speed serial cable connects the camera output to the PCI board. The board itself has a 2 MB memory which it uses as a buffer until the board has control of the computer's bus. The data in the buffer is transferred directly to the main memory of the computer at the bus top speed of the bus.

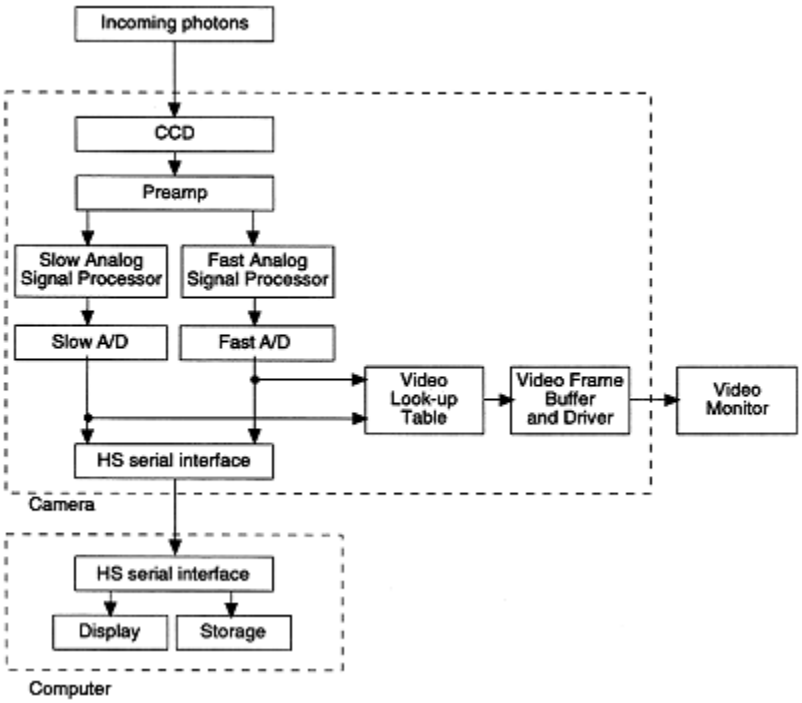

Figure 2.7. A block diagram of a CCD camera and computer interface.[29]

The PCI cable also allows control of specific hardware parameters within the camera, such as pixel binning and the selection of specific regions of interest within the imaging array.

B. The Power Supply

The power supply also acts as the temperature control box. Lower temperatures decrease the internal noise generated by the camera. The power supply is capable of displaying the actual temperature (Actual) the camera is operating at or the desired temperature (Set Point). Note that it is possible to set the camera to a temperature lower than what is actually possible to achieve. This will not damage the camera but will yield varying experimental results, because no final temperature has been established. Typically, the air cooled camera can achieve temperatures of -35°C and a few degrees cooler with liquid cooling.. The current system is air cooled and runs at -30°C.

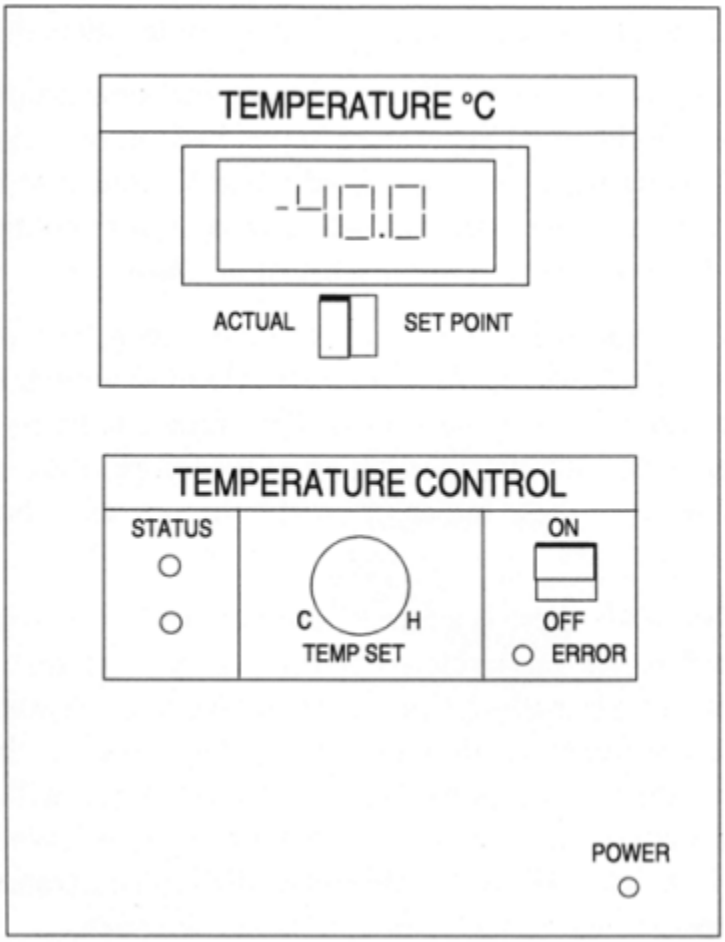

Figure 2.8. The front panel of the power supply.[29]

References:

1. Scientific Imaging Technologies, IN. An Introduction to Scientific Imaging Charge-Coupled Devices. SITe Products 1994.
2. Princeton Instruments Catalog, January, 1997