Improving Uintah's Scalability Through the Use of Portable Kokkos-Based Data Parallel Tasks

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ABSTRACT

The University of Utah's Carbon Capture Multidisciplinary Simulation Center (CCMSC) is using the Uintah Computational Framework to predict performance of a 1000 MWe ultra-supercritical clean coal boiler. The center aims to utilize the Intel Xeon Phi-based DOE systems, Theta and Aurora, through the Aurora Early Science Program by using the Kokkos C++ library to enable node-level performance portability. This paper describes infrastructure advancements and portability improvements made possible by our integration of Kokkos within Uintah. Scalability results are presented that compare serial and data parallel task execution models for a challenging radiative heat transfer calculation, central to the center's predictive boiler simulations. These results demonstrate both good strong-scaling characteristics to 256 Knights Landing (KNL) processors on the NSF Stampede system, and show the KNL-based calculation to compete with prior GPU-based results for the same calculation.

CCS CONCEPTS

•Hardware →Emerging technologies; **•Computer systems organization** →Parallel architectures; **•Computing methodologies** →Parallel computing methodologies; **•Applied computing** →Physical sciences and engineering;

KEYWORDS

Hybrid Parallelism, Kokkos, Knights Landing, Many-Core, MIC, Parallel, Portability, Radiation Modeling, Reverse Monte-Carlo Ray Tracing, Scalability, Stampede, Uintah, Xeon Phi

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1 INTRODUCTION

This study is motivated by the University of Utah's participation in the DOE/NNSA's Predictive Science Academic Alliance Program (PSAAP) II initiative. For this project, the University of Utah's Carbon Capture Multidisciplinary Simulation Center (CCMSC) has been using large-scale simulation to predict performance of a next-generation, 1000 MWe ultra-supercritical clean coal boiler. These predictions support the design and evaluation of an existing boiler, which has been developed by Alstom (GE) Power.

CCMSC predictive boiler simulations have been made possible through the use of the Uintah Computational Framework [4] and large high-performance computing (HPC) systems such as the NSF Stampede system and the DOE Mira and Titan systems. Looking ahead, the next phase of simulations will utilize the DOE Theta [9] and Aurora [8] systems through participation in the Aurora Early Science Program. Theta is a 9.65 petaFLOPS many-core system featuring 3,624 nodes based on Intel's second-generation Xeon Phi processor, Knights Landing. Aurora is a next-generation many-core system set to feature upwards of 50,000 nodes based on Intel's forthcoming third-generation Xeon Phi processor, Knights Hill.

The Intel Xeon Phi is a many-core device based on Intel's Many Integrated Core (MIC) Architecture. This architecture delivers high degrees of parallelism by presently offering up to 72 out-of-order cores featuring 4-way hyper-threading and 512-bit SIMD instructions. The latest generation Xeon Phi processor, Knights Landing, is binary compatible with past generations of Intel processors. Though easy to start using, the Xeon Phi poses new challenges for Uintah by requiring greater attention to data movement, thread-scalability, and vectorization to achieve performance. Early studies exploring Uintah's performance on first-generation Xeon Phi coprocessors, Knights Corner, have helped demonstrate some of these challenges [10, 19, 20].

For GPU-based systems, NVIDIA CUDA-based data parallel tasks have been introduced within Uintah [12, 13]. However, Uintah's existing serial tasks are still being used for MIC-based HPC systems. This poses challenges due to the large core/thread counts offered by the Xeon Phi. Though suitable for CPU-based HPC systems, Uintah's parallel execution of serial tasks within an MPI process is not viable for large-scale simulations on MIC-based HPC systems.

This challenge is addressed by using the Kokkos C++ library [7] within Uintah's infrastructure. Within an MPI process, the underlying Kokkos back-ends allow data parallel tasks to run on CPU-, GPU-, and MIC-based architectures. For MIC-based systems, this has helped overcome a scalability barrier pertaining to strict domain decomposition requirements. This has allowed us to achieve goos strong-scaling characteristics to 256 Knights Landing processors with Uintah's reverse Monte-Carlo ray tracing-based radiation model, more on which will be discussed in Section 3.

The remainder of this paper is structured as follows. Section 2 provides an overview of the Uintah Computational Framework. Section 3 introduces Uintah's reverse Monte-Carlo ray tracing-based radiation model, RMCRT. Section 4 describes the integration of the Kokkos C++ library within Uintah. Section 5 details the evolution of Uintah's MPI+X hybrid parallelism approach. Section 6 presents strong-scaling results gathered on Knights Landing processors in the NFS Stampede system. Section 7 outlines related work and section 8 concludes this paper.

2 THE UINTAH COMPUTATIONAL FRAMEWORK

The open-source (MIT License) Uintah Computational Framework consists of a set of simulation components and libraries enabling the simulation and analysis of complex chemical and physical reactions. These reactions are modeled by solving partial differential equations on structured adaptive mesh refinement grids. This framework was originally developed as part of the University of Utah's Center for the Simulation of Accidental Fires and Explosions (C-SAFE) initiative in 1997. Since then, Uintah has been widely ported and used to develop novel techniques for understanding a broad set of fluid-structure interaction problems. [3]

Though small-scale simulations are supported, Uintah emphasizes scalability across some of the largest HPC systems available today. Recent studies have demonstrated good scaling characteristics to 96K, 262K, and 512K CPU cores on the NSF Stampede, DOE Titan, and DOE Mira systems, respectively [3, 11, 20]. For Intel Xeon Phi-based systems, recent studies have demonstrated good strong-scaling characteristics to 16 Knights Corner coprocessors on the NSF Stampede system [19]. For the target application, recent studies have demonstrated good strong-scaling characteristics to 262K CPU cores [11] and 16K GPUs [13] on the DOE Titan system. The work presented here extends this by demonstrating good strong-scaling characterics to 256 Knights Landing processors on the NSF Stampede system.

Released in January of 2015, Uintah release 1.6.0 features four primary simulation components:

- *ARCHES*: This component targets the simulation of turbulent reacting flows with participating media radiation, more on which will be discussed in Section 3.
- *ICE*: This component targets the simulation of both low-speed and high-speed compressible flows.
- *MPM*: This component targets the simulation of multi-material, particle-based structural mechanics.
- *MPM-ICE*: This component corresponds to the combination of the ICE and MPM components for the simulation of fluid-structure interactions.

3 RADIATION MODELING WITHIN UINTAH

The CCMSC uses the ARCHES turbulent combustion simulation component for its predictive boiler simulations. In these simulations, radiation is the dominant mode of heat transfer and consumes a majority of compute time per timestep. At large scale, additional simulation challenges are faced due to the global, all-to-all nature of radiation [11].

ARCHES is a three-dimensional Large Eddy Simulation (LES) code described further in [25]. This code leverages a low-Mach number (M <0.3), variable density formulation to model heat, mass, and momentum transport in reacting flows. ARCHES was initially developed using the parallel discrete ordinates method [16] and P1 approximation [17] to solve the radiative transport equation. Though scalable, this approach resulted in solution of the associated sparse linear systems being the main computational cost for reacting flow simulations.

To reduce this cost, attention has been given to potentially more efficient reverse Monte-Carlo ray tracing (RMCRT) methods [14, 26]. This has led to the development of a stand-alone RMCRT-based radiation model suitable for use within Uintah's simulation components [12]. With Monte-Carlo ray tracing methods (forward or backward), two approaches are considered to parallelize the computation for structured grids: (1) parallelize by patch-based domain decomposition with local information only and pass ray information at patch boundaries via MPI, and (2) parallelize by patch-based domain decomposition with global information and reconstruct the domain for the quantities of interest on each node by passing domain information via MPI [11]. For the CCMSC's predictive boiler simulations, the first approach becomes intractable due to the ray counts used. These ray counts are orders of magnitude larger than those used to produce these results, which were between 209.5 million and 13.5 billion rays.

In the second approach, the primary difficulty is efficiently constructing the global information for millions of cells in a spatially decomposed (patch-based) domain. With this approach, an all-to-all communication phase is incurred for the radiative properties across the computational domain. Uintah has adopted the second RMCRT parallelization approach, providing global reconstruction of the radiative properties on each node to enabled local ray tracing. This model has since been (1) extended to support adaptive mesh refinement (AMR) to achieve scalability by reducing communication volume and computational complexity [11], (2) further adapted to run on GPUs at large-scale using this novel AMR approach [13], and (3) used to explore performance on the Knights Corner coprocessor [10]. Uintah offers multiple RMCRT-based radiation modeling approaches, ranging from a single-level approach to the AMR approach used in [11] and [13].

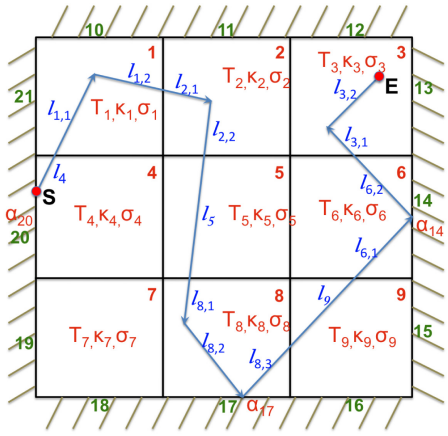

Figure 1: Two-dimensional outline of reverse Monte-Carlo ray tracing for the single-level approach. [12].

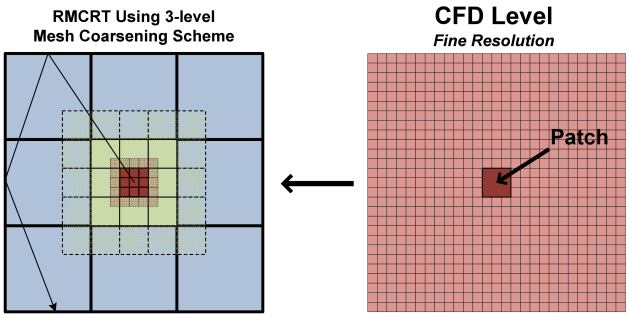

Figure 2: Two-dimensional outline of reverse Monte-Carlo ray tracing for a 3-level mesh refinement approach, illustrating how rays from a fine-level patch (right) may be traced across a coarsened domain (left) [11].

RMCRT uses random walks to model radiative heat transfer by tracing rays in reverse, *towards* their origin. During traversal, the amount of incoming radiative intensity absorbed by the emitter is computed to aid in solving the radiative transport equation. Figure 1 depicts how a ray is traced backwards from **S** to the emitter, **E**, for single-level RMCRT in a structured grid. Figure 2 depicts how ray traversal might be accomplished when using a 3-level mesh coarsening scheme.

RMCRT lends itself to scalable parallelism by allowing multiple rays to be traced simultaneously at any given cell and/or timestep. Additionally, RMCRT eliminates the need to trace rays that may never reach an origin. However, RMCRT does not eliminate the global, all-to-all nature of radiation. Within Uintah, RMCRT has been parallelized by spatially decomposing the computational domain into patches and tracing rays within a given patch to termination.

As new architectures are introduced within HPC systems, it is important for these RMCRT-based radiation modeling approaches to be portable. Uintah presently maintains separate CPU- and GPU-based implementations. However, this is cumbersome as it requires radiation model changes to be updated across two implementations. The introduction of a Kokkos-based implementation marks a step towards consolidating RMCRT-based radiation modeling approaches to a single implementation.

The results presented within this paper utilized the following implementations of RMCRT:

- Single-Level RMCRT:CPU
- Single-Level RMCRT:Kokkos
- 2-Level RMCRT:CPU
- 2-Level RMCRT:GPU
- 2-Level RMCRT:Kokkos

4 INCREMENTAL INTEGRATION OF KOKKOS

The Kokkos C++ library [7] is being used to avoid possible code bifurcation when extending Uintah to accelerators and many-core devices. Kokkos reduces the gap between development time and our ability to run on newly introduced systems by enabling performance portability. Here, performance portability refers to the maximization of portability across diverse architectures while striving to achieve performance comparable to hand-tuned code. For these advantages, Kokkos is believed to play a critical role in preparing Uintah for future HPC systems.

Developed by Sandia National Laboratories, Kokkos allows developers to write portable, thread-scalable code optimized for CPU, GPU, or MIC-based architectures. This library provides developers with data structures and architecture-aware parallel algorithms (e.g. *parallel_for*, *parallel_reduce*, and *parallel_scan*). When using these tools, Kokkos selects the memory layout and iteration scheme to utilize for a target architecture at compile time. This is enabled through various back-ends, which currently support NVIDIA CUDA, OpenMP, and PThreads programming models. Detailed usage information and demonstrations of performance portability can be found within [6].

As a large existing code base, Uintah must be extended incrementally. An overview of how this may be accomplished has been provided in [27]. To begin our integration, the first step was to incorporate support for Kokkos parallel loops within Uintah's infrastructure. This starting point was chosen to allow application developers to refactor code while simultaneously incorporating Kokkos further within Uintah's infrastructure. Results from early refactoring efforts [22, 27] have been encouraging, motivating our wider-spread integration of Kokkos. Next steps presently underway include the integration of Kokkos parallel loops within ARCHES, addition of support for Kokkos data structures, and further refinement of Uintah's hybrid parallelism approach.

5 EVOLUTION OF UINTAH'S HYBRID PARALLELISM APPROACH

Introduced within [18], the multi-threaded MPI scheduler marks Uintah's adoption of hybrid parallelism. Here, hybrid parallelism refers to the MPI+X programming model, where MPI is used for distributed memory parallelism and X (e.g. OpenMP, PThreads, etc) is used for shared memory parallelism. The work in [18] used MPI+PThreads to overcome scalability barriers imposed by memory footprint limitations on the NSF Kraken system and the DOE Jaguar system. In a similar sense, MIC-specific scalability barriers

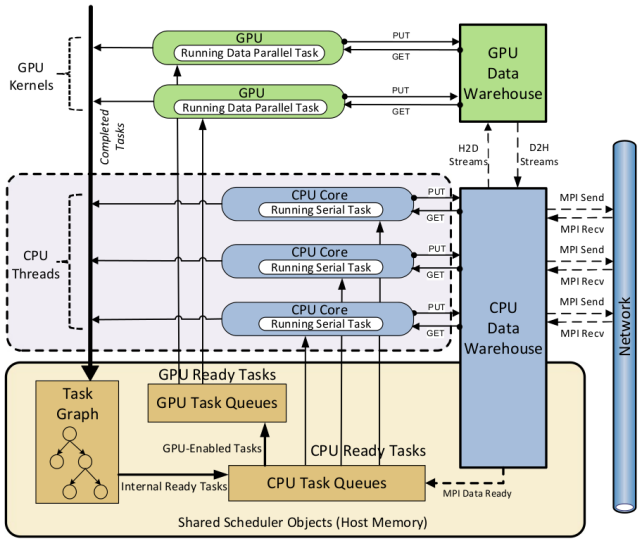

Figure 3: Uintah's multi-threaded MPI scheduler.

have necessitated the improvement of Uintah's hybrid parallelism approach.

Figure 3 presents an overview of Uintah's multi-threaded MPI scheduler. Within an MPI process, this scheduler uses several PThreads-based worker threads to execute tasks in parallel. For GPU-based architectures, worker threads execute NVIDIA CUDA-based data parallel tasks. For CPU-based architectures, worker threads execute serial tasks. For MIC-based architectures, worker threads can be used to execute Uintah's existing serial tasks. However, this is not conducive to scalability on many-core systems as will be demonstrated in Section 6.

With past CPU-based simulations, the largest core/thread counts that we have encountered within a node were 16 cores featuring 4 hardware threads on the DOE Mira system. The NSF Stampede system exceeds this by offering 68 cores featuring 4 hardware threads on a Knights Landing node. Though serial tasks have suited CPU-based architectures well, they are undesirable for many-core systems given this increase in core/thread counts. This holds due to the associated domain decomposition requirements. To utilize more worker threads within an MPI process, the computational domain must be subdivided to create an additional patches for each new worker thread.

To address this scalability barrier in a portable manner, Kokkos has been introduced within Uintah's dynamic MPI scheduler, more on which can be found in [21]. This has enabled the serial execution of Kokkos-based data parallel tasks within an MPI process. Figure 4 demonstrates how a Kokkos-based data parallel task may be used when running on a Knights Landing node.

The serial execution of Kokkos-based data parallel tasks eliminates the need to create an additional patch for each thread used within an MPI process. This offers greater control over patch sizes when balancing local and global communications at scale. Additionally, these tasks offer a potential to improve node-level performance through better utilization of a microarchitecture. For the Knights Landing processor, data parallel tasks allow per-patch work to be

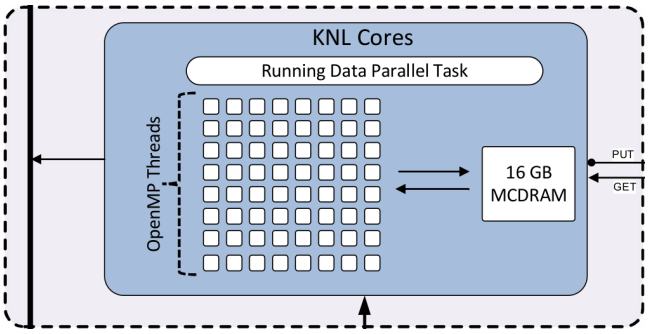

Figure 4: A Kokkos-based data parallel task, illustrating how a Knights Landing processor may be used at the node-level.

computed cooperatively using, for example, all hardware threads within a pair of cores, which share an L2 cache.

The preliminary RMCRT:Kokkos implementations utilized within this paper encapsulated the existing RMCRT:CPU tasks within a C++ functor to enable the use of Kokkos parallel algorithms. Once encapsulated, Uintah utilizes the OpenMP Kokkos back-end to enable data parallel tasks. As opposed to Uintah's worker thread scheduler, per-thread work is now scheduled dynamically by OpenMP.

6 STRONG-SCALING STUDIES

The strong-scaling studies presented within this section solve the Burns and Christen benchmark problem described in [5] using the following implementations of RMCRT:

- *Single-Level RMCRT:CPU*: This is an existing implementation of single-level RMCRT written to use serial tasks.
- *Single-Level RMCRT:Kokkos*: This is a preliminary implementation of single-level RMCRT written to use Kokkos-based data parallel tasks.
- *2-Level RMCRT:CPU*: This is an existing implementation of 2-level RMCRT written to use serial tasks.
- *2-Level RMCRT:GPU*: This is an existing implementation of 2-level RMCRT written to use NVIDIA CUDA-based data parallel tasks.
- *2-Level RMCRT:Kokkos*: This is a preliminary implementation of 2-level RMCRT written to use Kokkos-based data parallel tasks.

With the exception of GPU-based results in Figure 7, these results have been gathered on the KNL Upgrade of the NSF Stampede system [28]. This portion of Stampede features the Intel Xeon Phi 7250 Knights Landing processor and offers a variety of memory and cluster mode configurations. These studies were conducted on Knights Landing processors configured for *Cache-Quadrant* mode. With this in mind, each problem size explored fits within the 16 GB memory footprint of MCDRAM.

Here, strong-scaling refers to the subdivision of a fixed size problem to support increasing node counts. A fixed number of patches was maintained per node and their size reduced to create additional patches for additional nodes. For simulations using serial tasks, patches were sized to enforce 1 patch per hardware thread. For simulations using data parallel tasks, patches were sized to

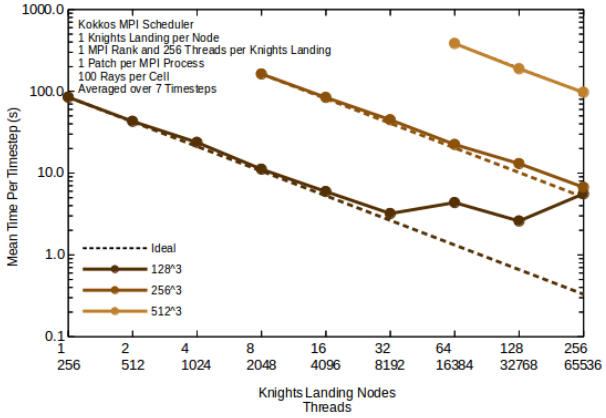

Figure 5: Strong-scaling results to 256 nodes for single-level RMCRT:Kokkos with data parallel tasks on Stampede's Knights Landing processors.

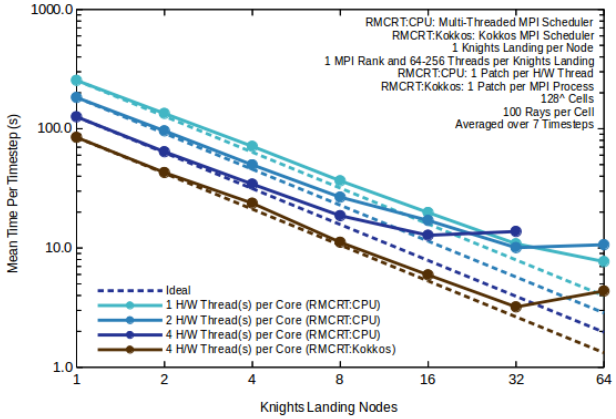

Figure 6: Strong-scaling results to 64 nodes for single-level RMCRT:CPU with serial tasks and single-level RMCRT:Kokkos with data parallel tasks on Stampede's Knights Landing processors.

enforce 1 patch per MPI process unless noted otherwise. For 2-level RMCRT simulations, coarse-level patch sizes were fixed and fine-level patch sizes were reduced as described above.

As a whole, simulations were launched using 1 MPI process per Knights Landing node. Within an MPI process, threads were launched in multiples of 64 to ease domain decomposition. For simulations using serial tasks, PThreads were launched without thread affinity. For simulations using data parallel tasks, OpenMP threads were launched via Kokkos with default affinity settings.

Figure 5 depicts strong-scaling results for single-level RMCRT:Kokkos. This implementation features serial execution of data parallel tasks within an MPI process. This figure presents results for three problem sizes (128^3, 256^3, and 512^3 cells). For each problem size, MPI processes were launched with 256 threads to utilize 4 hardware threads per core.

Figure 6 depicts strong-scaling results for single-level RMCRT:CPU. This implementation features parallel execution of serial tasks within an MPI process. This figure presents results for three thread counts (64, 128, and 256 threads per MPI process to utilize 1, 2, and 4 hardware threads per core, respectively). For each thread count, a problem size of 128^3 cells was utilized. To enable comparisons, this plot also features single-level RMCRT:Kokkos results from Figure 5 for the corresponding problem size and node counts.

Figure 7 depicts strong-scaling results for 2-level RMCRT:CPU. This implementation features parallel execution of serial tasks within an MPI process. This figure presents results for three problem sizes (128^3, 256^3, and 512^3 cells on the fine mesh with 32^3, 64^3, and 128^3 cells on the coarse mesh, respectively). For each problem size, MPI processes were launched with 256 threads to utilize 4 hardware threads per core. To enable comparisons, this plot also features prior 2-level RMCRT:GPU results gathered on the DOE NVIDIA Tesla K20X-based Titan system for the corresponding problem sizes and node counts. More details on 2-level RMCRT:GPU can be found in [13].

Figure 8 depicts strong-scaling results for 2-level RMCRT:Kokkos. This implementation features serial execution of data parallel tasks

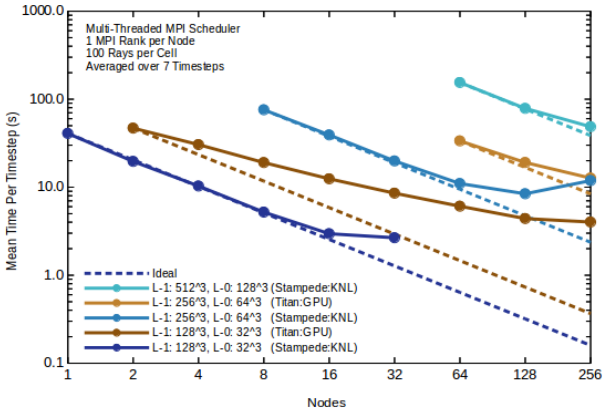

Figure 7: Strong-scaling results to 256 nodes for 2-level RMCRT:CPU with serial tasks on Stampede's Knights Landing processors and 2-level RMCRT:GPU with data parallel tasks on Titan's K20X GPUs.

within an MPI process. This figure presents results for two problem sizes (128^3 and 256^3 cells on the fine mesh with 32^3 and 128^3 cells on the coarse mesh, respectively). For each problem size, MPI processes were launched with 256 threads to utilize 4 hardware threads per core. To enable comparisons, this plot also features a portion of 2-level RMCRT:CPU results from Figure 7 for the corresponding problem sizes and node counts. For 2-level RMCRT:Kokkos, fine-level patches were sized to enforce 8 fine-level patches per MPI process.

Results presented within Figure 6 demonstrate that as more hardware threads were utilized per core, node-level performance increased at the expense of reductions in strong-scaling efficiency. This is attributed to the strict domain decomposition requirements imposed by the serial task execution model. Though it improved

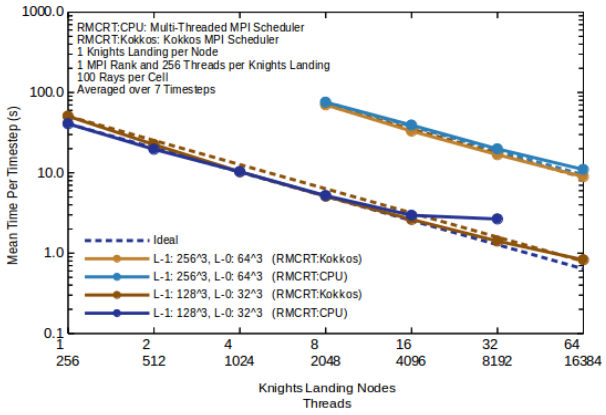

Figure 8: Strong-scaling results to 64 nodes for 2-level RMCRT:Kokkos with data parallel tasks and 2-level RMCRT:CPU with serial tasks on Stampede's Knights Landing processors.

node-level performance, the utilization of more threads per core required immediate reductions in patch size to accommodate additional threads within an MPI process. This expedited the breakdown of scalability, which is attributed to per-patch computation no longer sufficing to hide communication.

While this approach has suited CPU-based architectures well [11, 18], these observations suggest that serial tasks are undesirable for large-scale simulations on many-core systems. Supporting this conclusion, single-level RMCRT:Kokkos results included within Figure 6 suggest that we have overcome the scalability barrier posed by strict domain decomposition requirements through the use of data parallel tasks. This has been achieved with an accompanying improvement in node-level performance, which is believed to be attributed to improvements in microarchitecture utilization enabled via data parallel tasks.

Comparing results presented within Figure 5 to those within Figure 7, single-level RMCRT:Kokkos exhibited strong-scaling characteristics comparable to those of 2-level RMCRT:CPU. This is encouraging as the AMR approach utilized within 2-level RMCRT:CPU enabled strong-scaling characteristics to 262K CPU cores on the DOE Titan system that were previously unattainable via single-level RMCRT:CPU [11]. Further, node-level performance on Stampede's Knights Landing processors outperformed that of Titan's K20X GPUs. Though the K20X is dated, this is encouraging as Titan is one of the largest systems that we currently utilize. For upcoming Theta and Aurora simulations, this suggests a potential for improving boiler performance predictions through the use of finer mesh resolutions and/or more simulated time.

7 RELATED WORK

A collection of Knights Landing-specific material, including case studies, can found in [23]. An examination of Knights Landing memory and cluster modes on Stampede can be found in [24]. An analysis of Uintah and similar asynchronous many-task runtime systems (Charm++ [15] and Legion [1]) can be found in [2].

8 CONCLUSIONS AND FUTURE WORK

This work has helped advance Uintah's preparedness for large-scale simulations on many-core systems. Perhaps more important, it has improved our readiness for forthcoming simulations on the DOE Theta and Aurora systems. Such readiness encourages more productive use of our Aurora Early Science Program allocation when predicting boiler performance for the PSAAP II project.

These advancements have been made possible by our integration of Kokkos within Uintah. Though already supported for GPU-based architectures, Kokkos back-ends enable data parallel tasks for CPU- and MIC-based architectures. These data parallel tasks have helped overcome a MIC-specific scalability pertaining to strict domain decomposition requirements. The resulting flexibility in domain decomposition allows Uintah to accommodate larger thread counts within an MPI process and offers greater control over the balance between local and global communication. This has been accomplished by allowing MPI processes to utilize fewer, yet larger, patches, improving our ability to hide communication.

These results offer encouragement as we prepare to incorporate support for parallel execution of Kokkos-based data parallel tasks within an MPI process. By using Kokkos to improve Uintah's hybrid parallelism approach, we aim to increase Uintah's preparedness for a wider-range of HPC systems (e.g. the upcoming DOE NVIDIA Volta-based Summit system). This continued integration of Kokkos encourages better utilization of a node at the microarchitecture level while avoiding possible code bifurcation.

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